In re Patent Application of:
SFERRAZZA ET AL
Serial No. **10/686,362**
Filed: **OCTOBER 15, 2003**

REMARKS

The specification has been reviewed and editorial corrections have been effected, where appropriate, to make the specification consistent with the drawings. Reconsideration of this application in light of the foregoing amendments and following remarks is respectfully requested.

The rejection of Claims 1-15, under the provisions of 35 U.S.C. § 103, as being obvious over applicants' admitted prior art Figure 1 and the US patent to Massie 5,650,715 is respectfully traversed.

Before discussing the shortcomings of the prior art relied upon in the outstanding Office Action, the present invention will be briefly reviewed, in order that differences between the invention, particularly as delineated in Claims 1-15, and the prior art may be more readily appreciated.

As is described in the initial portions of the present specification beneath the heading "BACKGROUND OF THE INVENTION", it is a common place operation to place DC-DC power supplies into a sleep or quiescent mode when the user fails to manipulate an input output device within some prescribed period of time or closes the display lid of a personal computer. During this inactive or idle state, an auxiliary supply within the power control circuitry functions to keep only essential portions of the operational circuitry of the computer active, so as to minimize power consumption. Subsequently, when the user re-initiates use of the device, the power conservation circuit switches back to the main supply, which is customarily configured as a pulse width modulator based DC-DC converter.

In order to prevent misoperation of the device, it is necessary that the transition between the quiescent and active modes be as free of power rail anomalies as possible, which anomalies might otherwise affect the state of operation of a powered circuit device, such as a memory cell.

Applicants' Figure 1 shows one environment in which this occurs. During normal run or active mode, a charge is stored across an RC filter capacitor 31 as the feedback loop through the error amplifier 10 supplies a control input to the pulse width modulator driver circuitry 20. When the power supply transitions from the active mode to the quiescent or sleep mode, this charge begins to bleed off or discharge through the filter's resistor circuitry as normal operation of the error amplifier of the pulse width modulator circuit 20 is temporarily interrupted.

Eventually, when the power supply transitions out of its quiescent or sleep mode and back into the run mode, the discharged capacitor 31 will take some finite time to recharge as the pulse width modulator driver circuitry is active once again. During this interval, the output node undesirably supplies a voltage that is different from the correct value and appears to downstream powered devices as a power rail anomaly, which can cause misoperation of one or more devices.

The present invention circumvents this problem by controllably placing a sample and hold compensation circuit shown at 60 in Figure 2 of the drawings of the present application, in parallel with the AC compensation filter 30. This sample and hold compensation circuitry is operative, in response to a transition of the power supply from run mode to quiescent mode, to store and retain thereon a sampled voltage

that may be immediately available to the pulse width modulator driver circuitry at the termination of the sleep interval.

Figure 3 shows a preferred embodiment of the sample and hold-based, voltage compensation circuit, as a binary counter and a multi-stage current mirror coupled with a compensation differential amplifier 340.

In each of the independent claims presented for consideration, namely independent method Claim 1, upon which Claims 2-5 depend, independent Claim 6, upon which Claims 7-10 depend, as well as independent Claim 11, upon which Claims 12-15 depend, the above circuitry and operation of the present invention are concisely defined.

In Claim 1, for example, step (a) requires that in response to a transition in the operation of the DC-DC converter from run mode to quiescent mode, the voltage of an AC compensation filter is sampled and stored as a compensation voltage for an error amplifier of the DC-DC converter. Then, in response to a transition in the operation of a converter back from quiescent mode to run mode, this stored compensation voltage is coupled to drive circuitry of the DC-DC converter. A similar recitation is found in apparatus form in each of Claims 6 and 11.

Obviously, the prior art power supply circuitry shown in Figure 1 of the drawings of the present application does not include the sample and hold circuitry of the invention, since the problem occurs in the device of the type shown in Figure 1, and it is applicants who have discussed the problem and have provided a solution therefor.

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The US patent to Massie 5,650,715 neither addresses the problem nor the solution, so that it does not suggest any modification of the circuitry of Figure 1 upon which applicants' claims would read.

Instead, Massie is directed to a circuit for detecting peak current pulses on the secondary side of a transformer of a power supply and converting these peak current pulses into a DC voltage which can be used for various ancillary purposes, such as current limiting or current sharing, rather than being used to prevent an anomaly in the main control loop. Moreover, in Massie there is not switching of a DC-DC converter between quiescent and run modes.

The invention defined in applicants' Claims 1-15 is in a totally different field of DC-DC power supply circuitry, specifically in a non-isolated BUCK and linear power supply and deals with a dual mode supply (linear/PWM) configured circuit and the storage of the operating point of the control loop by way of a sample and hold of a voltage (not a peak current as in Massie) in order to minimize system perturbations when transitioning from the linear mode to the PWM mode of the DC-DC.

Simply put, there is no commonality between the circuitry of Massie and the circuitry of either Figure 1 of the drawings of the present application or the circuitry of the invention shown in Figures 2 and 3.

In addition to failing to address the fundamental operation and architecture of the present invention of the independent claims, Massie fails to disclose the particular architecture of the sample and hold circuitry, which applicants have claimed, including the incrementing of the

value of the comparison voltage and, in response to the comparison voltage equaling the voltage of the AC compensation filter, to terminate the incrementing of the value of the voltage and maintaining that comparison voltage by means of the unity gain amplifier as recited in Claim 3, for example, or the use of a counter with a current generator producing an output current proportional to the count value of the counter and coupling the output current to a summing resistor to realize the comparison voltage, as recited in Claim 5 and further dependent claims.

It is believed, upon reconsideration, it will be realized that the patent to Massie, which has its objective the detection of a peak current pulse, and does not address a solution to the problem of the circuitry of Figure 1 of the drawings of the present application, that it will be realized that the invention as defined in Claims 1-15 recites patentable subject matter, and therefore is in condition for allowance.

Favorable reconsideration of this application in light of the foregoing amendments and following remarks is, accordingly, earnestly solicited.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 01-0484 and please credit any excess fees to such deposit account.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number **703-872-9306** to MAIL STOP AMENDMENT, COMMISSIONER FOR PATENTS, this 27 day of April 2005.

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